REMARKS

Claims **1-5, 10-12 and 15-20** are pending in the present application after entry of the present amendment. Note claims 6-9 have been cancelled as being redundant. Claim 10 was objected to. Claim 16 was rejected under 35 U.S.C. 112. Claims 1-4 and 6-8 were rejected under 35 U.S.C. 102. Claims 1-12 and 15-16 were rejected under 35 U.S.C. 103. Claims 17-20 were allowed. While Applicant is grateful for the allowed claims, the Applicant respectfully traverses the pending rejections and objections.

Claim Objections

Applicant has made the grammatical change in claim 10 from "a control terminal having a clock signal" to "a control terminal receiving a clock signal." The change was made for a reason not related to patentability. The Applicant requests this objection be withdrawn.

Claim Rejections under 35 USC 112

Claim 16 was rejected under 35 U.S.C. 112 as being indefinite. Claims 15 and 16 have been amended to add a second control terminal and hence these rejections are requested to be withdrawn.

Claim Rejections under 35 USC 102

Claim 1 was rejected under 35 U.S.C. 102(b) as being anticipated by Gabara (U.S. Patent No. 6,018,260).

Claim 1 has been amended to recite, among other features: a differential input stage having differential third and fourth input terminals and complementary third and fourth output terminals connected to the first and second input terminals, respectively; another transistor having a current-handling terminal continuously connected to VSS and a gate connected to the third input terminal; and another cross coupled circuit including another cross coupled transistor having a gate

connected to the fourth output terminal. Gabara in Figure 2 shows only one differential input stage. Gabara does not disclose nor teach a differential input stage coupled to a differential output stage. Hence, this rejection should be withdrawn.

Claim 2 being dependent upon claim 1 should be allowable for at least the same reason claim 1 is allowable.

Claim 1 was also rejected under 35 U.S.C. 102(e) as being anticipated by Choe (U.S. Patent No. 6,373,292). In Figure 5 of Choe, there is a transistor, e.g., 52, between the input terminals and ground, which is turned on and off by a clock. Choe does not disclose nor teach another transistor having a current-handling terminal continuously connected to VSS and a gate connected to the third input terminal. Hence, this rejection should be withdrawn.

Claims 2-4, and 6-8 which depend upon claim 1 should be allowable for at least the same reason claim 1 is allowable.

Rejections under 35 U.S.C. 103

Claims 1-9 were rejected under 35 U.S.C. 103 as being unpatentable over Furuki (U.S. Patent No. 5,384,493) in view of Choe (U.S. Patent No. 6,373,292). In Figure 5 of Choe, there is a transistor, e.g., 52, between the input terminals and ground which is turned on and off by a clock. In Figure 6 of Furuki, there is a transistor, e.g., Q3 or Q4, between the input terminals and ground which is turned on and off by a clock. Both Furuki and Choe do not disclose nor teach another transistor having a current-handling terminal continuously connected to VSS and a gate connected to the third input terminal. Hence, this rejection should be withdrawn.

Claims 2-9 which depend upon claim 1 should be allowable for at least the same reason claim 1 is allowable.

Claim 10 was rejected under 35 U.S.C. 103 as being unpatentable over Hwang et. al. (U.S. Patent No. 5,777,491) in view of Choe (U.S. Patent No. 6,373,292). The Examiner combined the transistor 56 in Figure 2 of Choe with Figure 1 of

Hwang, by connecting the transistor 56 between nodes Q and QN of Figure 1 of Hwang. The Applicant respectfully disagrees that this combination is obvious to one of ordinary skill in the arts because the prior art cited by the Examiner, i.e., Choe and Gabara, teach away from this combination and the proposed modification changes the principle of operation of Hwang [MPEP 2143.01].

First, Choe (Figures 2 and 5) and Gabara (Figure 2) show that the first transistor 56 in Choe and 150 in Gabara is paired with a second transistor 52 in Choe and 120 in Gabara in order to periodically disconnecting the circuit from ground or VSS. Using Figure 2 of Choe as an example, the circuit in Figure 2 has a precharged stage and an evaluate stage. During the precharge stage, transistor 56 is on and transistor 52 is off. This means no current flows through transistors 46 and 48. OUT 58 and OUT_bar 60 settle at about the voltage of Vdd/2 [col. 2, lines 51- 63 of Choe]. During the evaluate stage, transistor 56 is off and transistor 52 is on. If In 54 is one, OUT 58 is discharged from Vdd/2 to ground, which turns transistor 44 on, which charges OUT_bar 60 from Vdd/2 to Vdd. Note transistor 42 is turned off [col. 2, line 64 to col. 3, line 10 of Choe].

The Examiner's stated that the purpose of transistor 56 in Choe is to reduce power consumption and improve speed of the circuitry. We disagree. At col. 2 lines 32-38 of Choe, the reason for reduced power is using a using a smaller supply voltage. Nothing in Choe discloses or suggests that using transistor 56 allows the use of a smaller supply voltage. In addition, both transistor 56 and transistor 52 allow faster output signal transitions [col. 3, lines 41-44 of Choe]. This is because in the precharge stage both OUT 58 and OUT_bar 60 are at Vdd/2 rather than Vdd or ground. This condition will not be true if transistor 52 were replaced with a direct connection to ground. In this case OUT 58 or OUT_bar 60 would be at ground during the precharge stage.

Hence, the prior art, i.e., Choe and Gabara, teach away from only using transistor 56 without using transistor 52. In other words, the prior art teaches that in combining transistor 56 of Choe across outputs Q and QN of Hwang, transistor 52 of Choe must be inserted between blocks 12 and 11 and ground of Hwang [see col. 1, line 66 to col. 2 line 3 of Hwang]. Hence, the combination of Choe with Hwang do not teach all the claim elements of claim 10.

Secondly, the Examiner's proposed modification changes the principle operation of Hwang. First, Figure 1 of Hwang has no clock. The transistor 56 of Choe is turned on and off periodically by a clock. Next, turning transistor 56 on in the circuit of Hwang, either clocked or unclocked, causes some very undesirable behavior and changes the principle operation of Hwang. In Figure 1 of Hwang any combination of A and/or B being one or zero will turn transistors N4 or N3 or both N1 and N2 on. This means that either Q or Qn will be pulled toward ground, as they are set to be equal by transistor 56 of Choe being turned on. Both P1 and P2 will be partially or fully turned on. Hence, there is a relatively large current flow through both legs of Figure 1 of Hwang during the precharge stage. Hence, the Applicant asserts that it would not be obvious to one of ordinary skill in the art to change an asynchronous circuit to a synchronous circuit with a large increase in power consumption during a precharge stage.

Hence, for at least the above reasons claim 10 should be allowable.

Claims 11-12 and 15-16 which depend upon claim 10 should be allowable for at least the same reasons claim 10 is allowable.

CONCLUSION

All claims should be now be in condition for allowance and a Notice of Allowance is respectfully requested.

If there are any questions, the applicant's attorney can be reached at Tel: 408-879-6149 (Pacific Standard Time).

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, Washington, D. C. 20231, on November 5, 2003.

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